Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An integrated circuit comprising:

a first input port for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries;

a second input port for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries;

a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and

a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time;

a controller configured to synchronize the first and second time-division multiplexed signals in response to the contents of the first and second frame position registers, wherein the controller is configured to generate first and second port-specific offset values in response to the contents of both the first and second frame position registers.

2. (original) The integrated circuit of claim 1 further comprising:

a first memory that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer; and

a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer.

3. (original) The integrated circuit of claim 1 further comprising:

a first retimer for retiming said first time-division multiplexed signal; and

a second retimer for retiming said second time-division multiplexed signal.

4. (original) The integrated circuit of claim 1 further comprising:

an output port; and

a cross-connect for outputting at least a portion of said first time-division multiplexed signal via said output port.

5. (currently amended) A method comprising:

receiving a first time-division multiplexed signal that comprises a first series of frame boundaries;

receiving a second time-division multiplexed signal that comprises a second series of frame boundaries;

indicating, at a point in time, how far said first time-division multiplexed signal is from a frame boundary;~~and~~

indicating, at said point in time, how far said second time-division multiplexed signal is from a frame boundary;

storing said first time-division multiplexed signal into a first memory at a location that is indicated by a first write pointer;

reading said first time-division multiplexed signal from a location in said first memory that is indicated by a first read pointer;

storing said second time-division multiplexed signal into a second memory at a location that is indicated by a second write pointer; and

reading said second time-division multiplexed signal from a location in said second memory that is indicated by a second read pointer; and

adjusting the first and second read pointers in response to first and second port-specific offset values that are generated in response to the indications of how far both the first and second time-division multiplexed signals are from their respective frame boundaries at said point in time.

6. (canceled)

7. (original) The method of claim 5 further comprising:

retiming said first time-division multiplexed signal in accordance with a clock signal; and

retiming said second time-division multiplexed signal in accordance with said clock signal.

8. (currently amended) An apparatus comprising:

a first integrated circuit comprising:

(i) a first input port for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries;

(ii) a second input port for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries;

(iii) a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and

(iv) a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time; and

a second integrated circuit comprising a controller for reading the contents of said first frame position register and said second frame position register;

wherein said first integrated circuit further comprises:

(v) a first memory that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer; and

(vi) a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that

reads said second time-division multiplexed signal at a location that is indicated by a second read pointer; and

wherein said controller is further configured to:

store a value in said first read pointer based on the contents of said first frame position register and said second frame position register;

synchronize the first and second time-division multiplexed signals in response to the contents of the first and second frame position registers;

generate first and second port-specific offset values in response to the contents of both the first and second frame position registers; and

adjust the first read pointer in response to the first port-specific offset value and the second read pointer in response to the second port-specific offset value.

9. (canceled)

10. (currently amended) The apparatus of claim 8 ~~9~~ wherein said first integrated circuit further comprises:

(vii) an output port; and

(viii) a cross-connect for outputting at least a portion of said first time-division multiplexed signal via said output port.

11. (currently amended) A composite switch comprising:

a first integrated circuit comprising:

(i) a first input port for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries;

(ii) a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and

a second integrated circuit comprising:

(i) a second input port for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries, and

(ii) a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time; and

a controller configured to:

~~for reading~~read the contents of said first frame position register and said second frame position register;

synchronize the first and second time-division multiplexed signals in response to the contents of the first and second frame position registers by:

generating first and second port-specific offset values in response to the contents of both the first and second frame position registers; and

adjusting the first read pointer in response to the first port-specific offset value and the second read pointer in response to the second port-specific offset value.

12. (canceled)

13. (previously presented) The composite switch of claim 11:

wherein said first integrated circuit further comprises:

(iii) a first memory that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer; and

wherein said second integrated circuit further comprises:

(iii) a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer.

14. (previously presented) The composite switch of claim 13 wherein said controller is further for storing a value in said first read pointer based on the contents of said first frame position register and said second frame position register.

15. (previously presented) A composite switch comprising:

a first integrated circuit for outputting a first time-division multiplexed signal that comprises a first series of frame boundaries to a second integrated circuit and for outputting a second time-division multiplexed signal that comprises a second series of frame boundaries to a third integrated circuit;

wherein said second integrated circuit comprises:

(i) a first input port for receiving said first time-division multiplexed signal,

(ii) a first memory that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer,

(iii) a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a first point in time, and

(iv) a first output port for outputting a third time-division multiplexed signal that is based on said first time-division multiplexed signal and that comprises a third series of frame boundaries;

wherein said third integrated circuit comprises:

(i) a second input port for receiving said second time-division multiplexed signal,

(ii) a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer,

(iii) a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary

in said second time-division multiplexed signal at said first point in time, and

(iv) a second output port for outputting a fourth time-division multiplexed signal that is based on said second time-division multiplexed signal and that comprises a fourth series of frame boundaries;

a fourth integrated circuit comprising:

(i) a third input port for receiving said third time-division multiplexed signal,

(ii) a third memory that stores said third time-division multiplexed signal at a location that is indicated by a third write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a third read pointer,

(iii) a third frame position register whose contents are related to how far said third time-division multiplexed signal is from a frame boundary in said third time-division multiplexed signal at a second point in time,

(iv) a fourth input port for receiving said fourth time-division multiplexed signal;

(v) a fourth memory that stores said fourth time-division multiplexed signal at a location that is indicated by a fourth write pointer and that reads said fourth time-division multiplexed signal at a location that is indicated by a fourth read pointer,

(vi) a fourth frame position register whose contents are related to how far said fourth time-division multiplexed signal is from a frame boundary in said fourth time-division multiplexed signal at said second point in time; and

a controller for reading the contents of said first frame position register and said second frame position register, for storing a value in said first read pointer based on the contents of said first frame position register and said second frame position register, for reading the contents of said third frame position register and said fourth frame position register, and for storing a value in said third read pointer based on the contents of said third frame position register and said fourth frame position register.

16. (previously presented) The composite switch of claim 15 wherein said first point in time and said second point in time are the same.

17. (canceled)

18. (canceled)

19. (currently amended) The integrated circuit of claim 1 ~~18~~ wherein the controller is further configured to adjust first and second read pointers in response to the first and second port-specific offset values, respectively.

20 - 26. (canceled)

27. (new) An integrated circuit comprising:

a first input port for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries;

a second input port for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries;

a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and

a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time;

a first memory that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer;

a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer;

a controller configured to adjust the first and second read pointers in response to the contents of the first and second frame position registers in order to synchronize the first and second time-division multiplexed signals; and

first and second frame position counters configured to count the number of words of said respective first and second time-division multiplexed signals received since a frame boundary.

28. (new) A method comprising:

transmitting a frame synchronization signal to frame position registers of multiple SONET/SDH switches;

reading contents of the frame position registers in response to the frame synchronization signal;

normalizing the contents of the frame position registers;

determining the largest propagation delay from the normalized contents of the frame position registers;

determining port-specific offsets for read pointer offset registers of the multiple SONET/SDH switches as a function of the longest propagation delay; and

writing the port-specific offsets into the read pointer offset registers.